CLAIMS

What is claimed is:

1. A switch matrix circuit comprising:

a plurality of switches organized in a row and column configuration; and

a current sensing circuit coupled to the plurality of switches, the current sensing circuit including a transistor and at least one resistor per column of the plurality of switches, wherein current amplified by the transistor and converted by the at least one resistor in a column is sensed as a logic level indicative of a switch status within the column for a selected row.

2. The switch matrix circuit of claim 1 wherein the transistor further comprises a bipolar junction transistor.

3. The switch matrix circuit of claim 1 wherein the row and column configuration further comprises an off-diagonal configuration having one switch per row and column intersection in all but one intersection per row.

4. The switch matrix circuit of claim 3 wherein each intersection lacking a switch lies in a different column within each row.

5. The switch matrix circuit of claim 4 wherein a single scan line supports providing a row input signal or reading a column output signal for one row and one column within the off-diagonal configuration.

6. The switch matrix circuit of claim 1 wherein a processor senses the switch status.

7. A circuit for more efficient switch selection sensing, the circuit comprising:

a switch matrix comprising a plurality of switches organized as a plurality of rows and columns;

a current sensing circuit coupled to the switch matrix; and

a processor coupled to the switch matrix and the current sensing circuit by a plurality of scan lines, wherein selection of a row by a scan line returns column current levels from the current sensing circuit to detect if a switch at a row and column intersection of the switch matrix has been selected.

8. The circuit of claim 7 wherein the plurality of scan lines further comprise a plurality of bi-directional scan lines wherein a single scan line provides both row selection and column sensing capabilities.

9. The circuit of claim 8 wherein the organization of the plurality of switches further comprise an off-diagonal organization to support the bi-directional scan lines.

10. The circuit of claim 7 wherein the current sensing circuit further comprises a transistor and resistor circuit for each column in the switch matrix.

11. The circuit of claim 10 wherein the column current levels indicate when the transistor is turned on and current passes through the resistor.

12. The circuit of claim 10 wherein the transistor further comprises a bipolar junction transistor.

13. A method for sensing switch status, the method comprising:

coupling a current sensing circuit to a switch matrix having a plurality of switches in a row and column configuration; and

utilizing a processor to detect switch status within the switch matrix based on current signals in the current sensing circuit.

14. The method of claim 13 further comprising forming the current sensing circuit as a transistor and at least one resistor per column of the plurality of switches.

15. The method of claim 14 wherein utilizing a processor to detect switch status further comprises detecting current amplified by the transistor and converted by the at least one resistor in a column as a logic level indicative of the switch status within the column for a selected row.

16. The method of claim 15 wherein utilizing a processor further comprises utilizing a plurality of bi-directional scan lines, wherein a single scan line provides both row selection and column sensing capabilities.

17. The method of claim 16 further comprising organizing the plurality of switches as an off-diagonal organization to support the bi-directional scan lines.

18. The method of claim 14 further comprising utilizing a bipolar junction transistor as the transistor.

19. A switch matrix circuit comprising:

a plurality of switches organized in a row and column off-diagonal configuration having one switch per row and column intersection in all but one intersection per row; and

a plurality of scan lines comprising a plurality of bi-directional scan lines, wherein a single scan line provides both row selection and column sensing capabilities for switch selection identification.

20. The switch matrix of claim 19 wherein the one intersection per row lacking a switch lies in a different column within each row.

21. The switch matrix of claim 19 wherein an analog to digital converter senses a switch status.

22. The switch matrix of claim 19 further comprising a diode and resistor circuit for each scan line.

23. A circuit for more efficient switch selection sensing, the circuit comprising:

a switch matrix including

a plurality of switches organized as a plurality of rows and columns; and

a plurality of resistors, each of the resistors electrically coupled in series with an associated one of the plurality of switches;

a voltage threshold sensing circuit coupled to the switch matrix by a plurality of scan lines; and

a processor coupled to the voltage threshold sensing circuit by a signal bus, wherein selection of a row by a scan line returns column voltage levels from the switch matrix to detect if a switch at a row and column intersection of the switch matrix has been selected.

24. The circuit of claim 22 wherein the voltage threshold sensing circuit converts the column voltage levels to logic states.

25. The circuit of claim 24 wherein the voltage threshold sensing circuit includes an analog to digital converter.

26. The circuit of claim 24 wherein the voltage threshold sensing circuit includes a voltage level converter including a transistor.